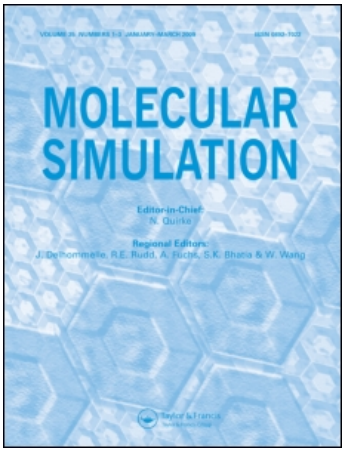

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A complete analytic surface potential-based core model for intrinsic nanowire surrounding-gate MOSFETs

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A complete analytic surface potential-based core model for intrinsic nanowire surrounding-gate MOSFETs

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An analytic surface potential-based non-charge-sheet core model for intrinsic nanowire surrounding-gate (SRG) MOSFETs is presented in this paper. Starting from the Poisson–Boltzmann equation in the cylindrical SRG MOSFETs, a surface potential equation is derived. Based on the exact surface potential solutions evaluated at the source and drain ends, a single set of the analytic drain current expression is obtained from the Pao–Sah's dual integral without the charge-sheet approximation. The analytical trans-capacitance model is also obtained from Ward–Dutton's charge partition method within the surface potential-based model framework. It is shown that the proposed drain current model and trans-capacitance model are valid for all operation regions, allowing the nanowire SRG MOSFET characteristics to be adequately described from the linear to saturation and from the sub-threshold to strong inversion region without any fitting-parameters. Moreover, the model prediction is verified by the three-dimensional numerical simulation.

Keywords: non-classical MOS transistor; surrounding-gate MOSFETs; device physics; surface potential model; non-charge-sheet approximation

1. Introduction

According to ITRS [1], continuous scaling down of the traditional single-gate (SG) bulk Complementary Metal Oxide Semiconductor (CMOS) will soon hit its limit imposed by short channel effects and severe gate oxide tunnelling. In order to extend CMOS performance to or beyond 10 nm technical generation, various nanoscale molecular materials and devices, as promising building blocks of nanoelectronics in the future, are also being widely studied [2,3]. Among the emerging non-planar devices structures, nanowire surrounding-gate (SRG) MOSFETs are allowed to shrink to the smallest gate length due to their stronger gate control over the channel [4,5].

In parallel with process technology advance [6–8], understanding the device physics and developing the corresponding compact models of silicon nanowire SRG MOSFETs are highly important for nanowire based circuit application and beneficial to other molecular device research. Extensive studies on nanowire SRG MOSFET modelling have been performed in recent years and the related device physics have been well described by many different models [9–21]. In the potential-based SRG MOSFET models, the closed-form current models are expressed in terms of the intermediate variables or the potentials of the surface and centric point at the source and drain ends [11,13]. In the charge-based SRG MOSFET models, the inversion charge model is developed for the SRG MOSFETs based on a smooth function and interpolation [14–17]. In addition, a carrier-based approach is found to be useful in developing a generic compact model for SRG MOSFETs [18,19]. On the other hand, we also noted that considerable attention has been focused on developing surface potential-based models in recent compact model formulations [20,21]. At present, there is a general consensus that the surface potential approach not only includes as much device physics as possible but also retains high accuracy and continuity.

Under such a background, an analytical surface potential-based non-charge-sheet core model is developed to simulate the drain current and trans-capacitance characteristics of the intrinsic nanowire SRG MOSFETs in this paper. The proposed drain current model is based on the closed-form solution of Poisson–Boltzmann equation and Pao–Sah's dual integral drift and diffusion equation [22]. We demonstrate in this paper that an analogous formulation as proposed by Brews [23] for the SG bulk MOSFET can be carried out for the intrinsic nanowire

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SRG MOSFETs. The model has three distinctive features: (i) a single set of the surface potential voltage equation is obtained from the exact Poisson–Boltzmann equation solution in the intrinsic SRG MOSFET structure, similar to that of the bulk MOSFETs, for which the complete surface potential equation is the beginning to develop a continuous model; (ii) the drain current model, obtained from the Pao–Sah's dual integral, is described by one continuous function in terms of the surface potentials at the source and drain ends, tracing properly the transition between different SRG MOSFET operation regions without resorting to any non-physical fitting-parameters; (iii) the charge-sheet approximation, typically used in bulk MOSFET models to simplify the Pao–Sah's double integral for the current [22,23], is not invoked, properly capturing the volume inversion effect in SRG MOSFETs. The analytical trans-capacitance model within the surface potential-based model framework is also obtained from Ward–Dutton's charge partition method. In order to complete the model, short-channel effects, quantum effects, low and high field transport and more will be added in the near future.

2. Model development

An ideal long channel SRG MOSFET without advanced effects, such as quantum confinement, short channel effects, drain induced barrier lowering and velocity saturation, is considered in this paper for simplicity. It will be possible to incorporate these effects into a complete nanowire SRG MOSFET model in the near future after the core model is fully developed. The coordinate system used in this work is shown in Figure 1 with r representing the radial distance from the centre of the channel and R being the radius of the cylindrical structure. It also assumes that the quasi-Fermi level is constant in the radial direction, so that the current flows only along the channel (y-direction). The energy levels are referenced to the electron quasi-Fermi level of the source end since there is no body contact in the intrinsic nanowire SRG MOSFETs.

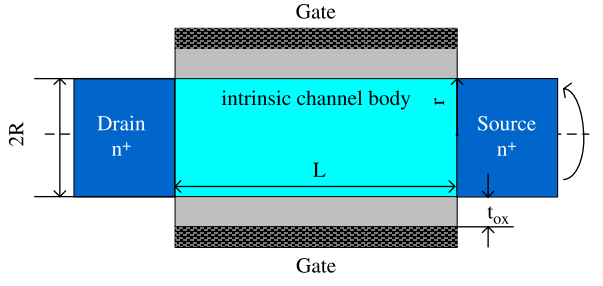

Figure 1. Schematic diagram and coordinate of an intrinsic nanowire SRG MOSFET.

2.1 Surface potential equation derivation

Following the gradual-channel approximation, Poisson's equation takes the one-dimensional form

$$\frac{\mathrm{d}^2\phi}{\mathrm{d}r^2}+\frac{1}{r}\frac{\mathrm{d}\phi}{\mathrm{d}r}=\frac{kT}{qL_i^2}\mathrm{e}^{q(\phi-V)/kT}, \tag{1}$$

where all symbols have their common physics meanings: ϕ, the electrostatic potential; V, the quasi-Fermi-potential with $V=0$ at the source and $V=V_{\mathrm{ds}}$ at the drain end; $L_i^2=\varepsilon_{\mathrm{si}}kT/q^2n_i$ is the square of the intrinsic silicon Debye length; n_i, the silicon intrinsic carrier concentration.

Note that $\phi \gg kT/q$ is assumed in (1) and the hole density is neglected since only an nMOSFET is considered here. The electrostatic potential and electric field satisfies the following boundary conditions at the surface and centric point for the coordinate choice:

$$\left.\frac{\mathrm{d}\phi}{\mathrm{d}r}\right|_{r=0}=0,\quad \phi|_{r=R}=\phi_{\mathrm{s}},\quad \phi|_{r=0}=\phi_0. \tag{2}$$

Then Equation (1) can be analytically solved yielding [11,12]

$$\phi_{\mathrm{s}}=\phi_0-\frac{2kT}{q}\ln\left[1-\frac{R^2}{8L_i^2}\exp\left[\frac{q(\phi_0-V)}{kT}\right]\right] \tag{3}$$

and

$$\left.\frac{\mathrm{d}\phi}{\mathrm{d}r}\right|_{r=R}=\frac{RkT}{2qL_i^2}\exp\left[\frac{q(\phi_0-V)}{kT}\right]\Big/\left[1-\frac{R^2}{8L_i^2}\exp\left[\frac{q(\phi_0-V)}{kT}\right]\right]. \tag{4}$$

From Gauss's law, the following relationship exists between the charge, surface potential and the gate voltage

$$C_{\mathrm{ox}}(V_{\mathrm{gs}}-\Delta\varphi-\phi_{\mathrm{s}})=\varepsilon_{\mathrm{si}}\left.\frac{\mathrm{d}\phi}{\mathrm{d}r}\right|_{r=R}, \tag{5}$$

where $C_{\mathrm{ox}}=\varepsilon_{\mathrm{ox}}/[R\ln(1+t_{\mathrm{ox}}/R)]$ is the gate oxide capacitance and $\Delta\varphi$ is the work-function difference between the gate and intrinsic silicon.

Substituting the results from (3) and (4) into (5) leads to

$$C_{\mathrm{ox}}(V_{\mathrm{gs}}-\Delta\varphi-\phi_{\mathrm{s}})= \times\frac{\sqrt{2}\varepsilon_{\mathrm{si}}kT}{qL_i}\exp\left[\frac{q(\phi_{\mathrm{s}}-V)}{2kT}\right]\sqrt{1-\exp\left[-\frac{q(\phi_{\mathrm{s}}-\phi_0)}{2kT}\right]}. \tag{6}$$

Moreover, substituting (3) into (6) leads to

$$C_{ox}(V_{gs} - \Delta\varphi - \phi_s) = \frac{R\varepsilon_{si}kT}{2qL_i^2} \exp\left[\frac{q(\phi_s + \phi_0 - 2V)}{2kT}\right]. \tag{7}$$

From (7), we obtain the centric potential expression

$$\phi_0 = 2\,\mathrm{V} - \phi_s + \frac{2kT}{q} \ln\left[\frac{2L_i^2 C_{ox} q(V_{gs} - \Delta\varphi - \phi_s)}{R\varepsilon_{si}kT}\right]. \tag{8}$$

Then (8) is substituted back into (3), so we have

$$\frac{q(V_{gs} - \Delta\varphi - \phi_s)e^{-q(\phi_s - V)/kT}}{kT}\left[\frac{1}{R} + \frac{qC_{ox}(V_{gs} - \Delta\varphi - \phi_s)}{4\varepsilon_{si}kT}\right] = \frac{\varepsilon_{si}}{2L_i^2 C_{ox}}. \tag{9}$$

Equation (9) is a quadratic equation with respect to $(V_{gs} - \Delta\varphi - \phi_s)$ and has two roots. However, from physics meaning of the solution, only one single root is reasonable

$$\frac{q(V_{gs} - \Delta\varphi - \phi_s)}{kT} = \frac{2\varepsilon_{si}}{RC_{ox}}\sqrt{1 + \frac{R^2}{2L_i^2}e^{q(\phi_s - V_{ch})/kT}} - \frac{2\varepsilon_{si}}{RC_{ox}}. \tag{10}$$

Equation (10) is a fully rigorous surface potential–voltage equation of the intrinsic nanowire SRG MOSFETs [12,13] that can be solved analytically by the similar method in [24] to get the accurate surface potential value for the given geometry and bias parameter. The basic derivations above have been published in [14,15].

2.2 Drain current model derivation

The quasi-Fermi potential V varies from the source to the drain. The functional dependence of $V(y)$ and $\phi_s(y)$ is determined by the current continuity equation. From the Pao–Sah's dual integral [22], integrating $I_{ds}dy$ from the source to the drain and expressing dV/dy as $(dV/d\phi_s)(d\phi_s/dy)$, the non-charge-sheet drain current of the SRG MOSFETs is written as

$$I_{ds} = \mu\frac{2\pi R}{L}\int_0^{V_{ds}} Q(V)\,dV = \mu\frac{2\pi R}{L}\int_{\phi_{ss}}^{\phi_{SL}} Q(\phi_s)\frac{dV}{d\phi_s}\,d\phi_s, \tag{11}$$

where ϕ_{SS}, ϕ_{SL} are the solutions to (10) corresponding to $V = 0$ and $V = V_{ds}$, respectively. The parameter μ is the effective mobility.

Notice that the total mobile charge per unit gate area $Q(\phi_s) = C_{ox}(V_{gs} - \Delta\varphi - \phi_s)$. The $dV/d\phi_s$ term in (11) can also be expressed as a function of ϕ_s by differentiating (9) that results in

$$\frac{dV}{d\phi_s} = 1 + \frac{1 + (C_{ox}R/2\varepsilon_{si})(q(V_{gs} - \Delta\varphi - \phi_s)/kT)}{(q(V_{gs} - \Delta\varphi - \phi_s)/kT)[1 + (C_{ox}R/4\varepsilon_{si})(q(V_{gs} - \Delta\phi - \phi_s)/kT)]}. \tag{12}$$

Substituting these two factors into (11), we have

$$I_{ds} = \frac{2\pi R\mu C_{ox}}{L}\int_{\phi_{SS}}^{\phi_{SL}}\left[(V_{gs} - \Delta\varphi - \phi_s) + \frac{2kT}{q} - \frac{kT}{q}\left(1 + \frac{C_{ox}qR(V_{gs} - \Delta\varphi - \phi_s)}{4\varepsilon_{si}kT}\right)^{-1}\right]d\phi_s. \tag{13}$$

The integration of (13) is performed analytically to yield

$$I_{ds} = \frac{2\pi R\mu C_{ox}}{L}[F(\phi_{SL}) - F(\phi_{SS})] \tag{14a}$$

with

$$F(\phi_s) = \left((V_{gs} - \Delta\varphi)\phi_s - \frac{\phi_s^2}{2}\right) + \frac{2kT\phi_s}{q} + \left(\frac{kT}{q}\right)^2\frac{4\varepsilon_{si}}{RC_{ox}}\ln\left(1 + \frac{C_{ox}qR(V_{gs} - \Delta\varphi - \phi_s)}{4\varepsilon_{si}kT}\right). \tag{14b}$$

With the surface potentials ϕ_{SS}, ϕ_{SL} solved from (10), the final drain current model is obtained without any fitting parameters. Actually, the formulation (14a,b) is in the equivalent form of Equation (38) in [13], but the derivation here is more straightforward and simple.

2.3 Capacitance model derivation

Based on the current continuity principle, all terminal charges and corresponding trans-capacitances can be derived analytically. Under ordinary bias conditions, the charges distribute non-uniformly in the channel except for the case of $V_{ds} = 0$. To account for this distribution character, various integral functions are invoked along the channel of a MOSFET [25]. Since there is no depletion charge for an intrinsic nanowire SRG MOSFET, the integration for the charge distribution function can be performed analytically. Here Q_g, Q_s and Q_d are used to denote the total gate, source and drain terminal charges for simplicity.

To calculate the terminal charges and intrinsic capacitances, we use the surface potential expression given in (10). Considering current continuity, the drain

current can be expressed as

$$I_{ds} = 2\pi R\mu Q_i(\phi_s)\frac{dV}{dy} = 2\pi R\mu_0 Q_i(\phi_s)\frac{dV}{d\phi_s}\frac{d\phi_s}{dy}. \quad (15)$$

Since current continuity requires the current to be constant along the channel, we can express the surface potential distribution as a function of the distance from the source in the channel. Here, a constant mobility is assumed. Substituting Equation (12) into (15) and performing the integral yield

$$\frac{y}{L} = \frac{F[\phi_s]|_{\phi_s}^{\phi_{SS}}}{F[\phi_s]|_{\phi_{SL}}^{\phi_{SS}}}. \quad (16)$$

In order to obtain the quasi-static terminal charges, the total inversion charge must be partitioned into a source portion and a drain portion. Here, we use Ward–Dutton's charge partition method [26] to define the stored charges at the source as

$$Q_s = \int_0^L Q\left(\frac{y}{L}\right) dy \quad (17)$$

and at the drain as

$$Q_d = \int_0^L Q\left(1 - \frac{y}{L}\right) dy, \quad (18)$$

respectively.

The integrals in (17) and (18) can be performed analytically. In the meantime, the total channel charge (or gate charge) can be obtained in terms of the surface potential in the silicon as

$$Q_g = \int_0^L Q\, dy. \quad (19)$$

Transforming the variable from y to ϕ_s in (19)

$$Q_g = \int_0^L Q\frac{dy}{d\phi_s}\, d\phi_s. \quad (20)$$

Substituting (16) and Q into Equation (20), the integral in (20) is performed analytically to yield

$$Q_g = 2\pi RLC_{ox}\left(\frac{kT}{q}\right)\frac{G[\phi_s]|_{\tilde{\phi}_{SL}}^{\tilde{\phi}_{ss}}}{F[\phi_s]|_{\phi_{SL}}^{\phi_{ss}}} \quad (21)$$

with

$$G(\phi_s) = \frac{1}{3}\tilde{\phi}_s^3 + \tilde{\phi}_s^2 - s\tilde{\phi}_s + s^2\ln(s + \tilde{\phi}_s), \quad (22)$$

where $\tilde{\phi}_s = q(V_{gs} - \Delta\varphi - \phi_s)/kT$, and $s = 4\varepsilon_{si}/RC_{ox}$.

Based on a similar procedure, the analytic source and drain terminal charges are obtained from (17) and (18) by transforming the variable from y to ϕ_s. The final results are given in (23) and (24):

$$Q_s = -2\pi RLC_{ox}\left(\frac{kT}{q}\right)\frac{F(\phi_{SL})G(\phi_s)|_{\phi_{SL}}^{\phi_{ss}} + M(\phi_s)|_{\phi_{SL}}^{\phi_{ss}}}{\left[F[\phi_s]|_{\phi_{SL}}^{\phi_{ss}}\right]^2} \quad (23)$$

and

$$Q_d = -2\pi RLC_{ox}\left(\frac{kT}{q}\right)\frac{F(\phi_{SS})G(\phi_s)|_{\phi_{ss}}^{\phi_{SL}} + M(\phi_s)|_{\phi_{ss}}^{\phi_{SL}}}{\left[F[\phi_s]|_{\phi_{SL}}^{\phi_{ss}}\right]^2} \quad (24)$$

with

$$\begin{aligned} M(\phi_s) = \frac{1}{2}\Bigg[&\frac{1}{90}\tilde{\phi}_s\left(-30s^3 + 15s^2\tilde{\phi}_s - 10s\tilde{\phi}_s(9 + \tilde{\phi}_s)\right.\\ &\left.+3\tilde{\phi}_s^2(80 + 45\tilde{\phi}_s + 6\tilde{\phi}_s^2)\right)\\ &+\frac{s}{3}\left(s^3 + 6s\tilde{\phi}_s - 2\tilde{\phi}_s^2(3 + \tilde{\phi}_s)\right)\ln(s + \tilde{\phi}_s)\\ &- s^3\ln^2(s + \tilde{\phi}_s)\Bigg]. \end{aligned} \quad (25)$$

From Equations (21), (23) and (24), all three terminal charges of nanowire SRG MOSFETs can be analytically calculated from ϕ_{SS} and ϕ_{SL}.

One important fact is that Equations (21), (23) and (24) are not directly available for the special case of $V_{ds} = 0$. It is easily noted that when $V_{ds} = 0$, both the numerator and denominator of the all charges become zero, which causes numerical instability when evaluating the charges. L'Hospital's rule is usually needed to carry on the calculation [19]. For this case, the inversion charge distribution is uniform along the channel direction since there is no current flow, thus, the gate terminal charge is directly written as

$$Q_g = 2\pi RLQ_i. \quad (26)$$

At the same time, the charge in the channel is equally partitioned between the source and drain. In order to avoid numerical instability, all terminal charge should be asymptotically equal to the value of the charge here as V_{ds} approaches zero.

The nanowire SRG MOSFET is essentially a three-terminal device, a nine-capacitance matrix is written as

$$C_{ij} = \begin{cases} \frac{\partial Q_i}{\partial V_j} & i = j \\ -\frac{\partial Q_i}{\partial V_j} & i \neq j \end{cases} = \begin{bmatrix} C_{ss} & C_{sd} & C_{SG} \\ C_{ds} & C_{dd} & C_{DG} \\ C_{gs} & C_{gd} & C_{gg} \end{bmatrix}. \quad (27)$$

With the analytical expressions of the three-terminal charges formulated, all capacitances are derived as a function of the surface potentials at the source and drain ends. The analytical expressions of all nine trans-capacitances can be simplified by using the dependency of the trans-capacitance matrix

$$C_{gg} + C_{sg} + C_{dg} = C_{gs} + C_{gd}, \quad (28)$$

$$C_{ss} + C_{sd} + C_{sg} = C_{gs} + C_{ds}, \quad (29)$$

$$C_{dd} + C_{sd} + C_{gd} = C_{ds} + C_{dg}. \quad (30)$$

In such a case, we only need to calculate four independent trans-capacitances while the others can be obtained directly from a linear combination of the calculated capacitances via Equations (28,29). For example, the gate capacitances are written as

$$C_{gg} = \frac{\partial Q_g}{\partial V_{gs}} = \frac{\partial Q_g}{\partial \phi_{SS}} \frac{\partial \phi_{SS}}{\partial V_{gs}} + \frac{\partial Q_g}{\partial \phi_{SL}} \frac{\partial \phi_{SL}}{\partial V_{gs}}, \quad (31)$$

$$C_{gs} = -\frac{\partial Q_g}{\partial V_s} = -\frac{\partial Q_g}{\partial \phi_{SS}} \frac{\partial \phi_{SS}}{\partial V_s} - \frac{\partial Q_g}{\partial \phi_{SL}} \frac{\partial \phi_{SL}}{\partial V_s}, \quad (32)$$

$$C_{gd} = -\frac{\partial Q_g}{\partial V_{ds}} = -\frac{\partial Q_g}{\partial \phi_{SL}} \frac{\partial \phi_{SL}}{\partial V_{ds}}. \quad (33)$$

The derivatives of $\partial Q_g/\partial \phi_{SL}$, $\partial Q_g/\partial \phi_{SS}$ are calculated from (21) while the derivatives of $\partial \phi_{SS}/\partial V_s$, $\partial \phi_{SS}/\partial V_{gs}$ and $\partial \phi_{SL}/\partial V_{ds}$, $\partial \phi_{SL}/\partial V_{gs}$ are obtained from Equation (10). It should be noted that $\partial \phi_{SS}/\partial V_{ds} = \partial \phi_{SL}/\partial V_s = 0$ since there is no short-channel effects involved in this discussion for simplicity.

Similarly, the drain capacitance and source capacitance can be finally expressed as the function of the surface potentials at the source and drain end. The final analytical expressions and these capacitance elements are too lengthy to show here, but they all are simple elementary functions. The remaining trans-capacitances are calculated from the capacitance relationship given in Equations (28–30).

3. Results and discussion

In the above section, the surface potential equation, drain current model and trans-capacitance model of a nanowire SRG MOSFETs are obtained in a closed-form. To test the validity of the proposed model, surface potential solutions, drain current and trans-capacitances from the analytic model are compared with three dimension numerical simulation results from Sentaurus Device [27]. In the following discussion, a channel length (L) of 1 μm, silicon oxide thickness (t_{ox}) of 2 nm and a mid-gap gate material are assumed unless specified. A constant effective mobility of 400 $cm^2/V\,s$ has been used for current calculations both in the model and in the simulation.

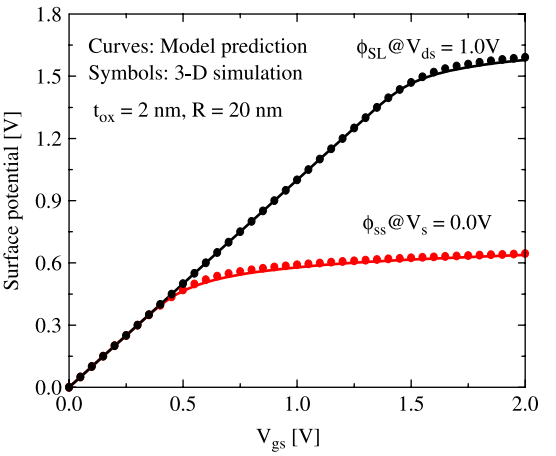

Figure 2. Comparison of source and drain end surface potentials obtained from (10) (solid curves) compared with the three dimension numerical result (symbols).

Figure 2 shows the surface potential versus gate voltage curves calculated from (10) for the source and drain ends in comparison with the three-dimensional simulation. The solution given by (10) is continuously and smoothly valid for all regions of the SRG MOSFET operation. It is found that the results from (10) shows an agreement with the three-dimensional simulation in all operation regions for both the source and drain potentials. Since surface potentials are lightly sensitive to the radii of intrinsic nanowire SRG MOSFET, only one geometry configuration is demonstrated in the figure.

Figure 3 illustrates the comparison of the inversion charge density between the model prediction and the three-dimensional simulation for different silicon body radii. It is observed from Figure 3 that the agreement between the model and simulation is very good. In addition, the sub-threshold charge increases with the increase of the silicon radius. The unique volume inversion effect is accurately predicted from the presented model, coinciding with the non-classical MOSFET device physics.

From (14a,b), the SRG MOSFET drain current can be easily computed. In the following, the SRG MOSFET operation regions are derived from this continuous surface potential-based analytical model:

i) *Linear region above threshold*. In this region the drift current component dominates the device performance. Hence, we observe that the total drain

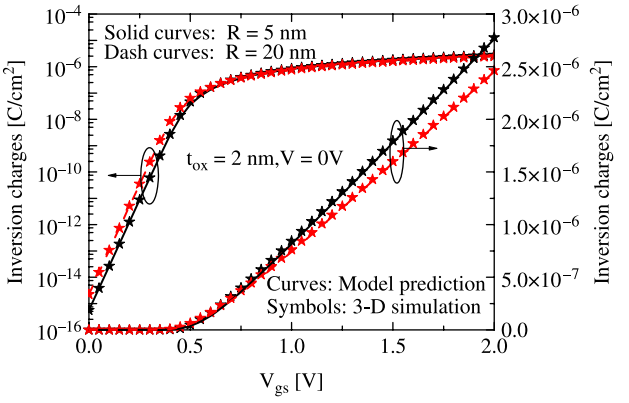

Figure 3. Inversion charge characteristics obtained from (5) (solid and dash curves) based on calculated surface potential, compared with the three dimension numerical simulation (symbols) for a given V_{gs}, ϕ_s can be solved from (10) as a function of V.

current can be approximated by first two terms only above the threshold as shown in (34):

$$I_{ds} \approx \frac{2\pi R\mu C_{ox}}{L}\left[(V_{gs}-\Delta\varphi)(\phi_{SL}-\phi_{SS})-\frac{1}{2}(\phi_{SL}^2-\phi_{SS}^2)\right]. \quad (34)$$

This current expression is just the drift component of the traditional surface potential-based bulk MOSFET current models, thus dominates in the strong inversion region. As mentioned above, the surface potential in this strong inversion region is not sensitive to the radius, indicating that the drain current is just in proportion to the radius of the nanowire SRG MOSFET.

ii) *Sub-threshold region*. Below threshold voltage the SRG MOSFET current picture has a little difference from the bulk MOSFET model. Here, the first two components are negligible in this region. As a result, the total drain current is described by

$$I_{ds} \approx \frac{2\pi R\mu C_{ox}}{L}\left[\frac{2kT}{q}(\phi_{SL}-\phi_{SS}) + \left(\frac{kT}{q}\right)^2\frac{4\varepsilon_{si}}{RC_{ox}}\ln\left[\frac{4\varepsilon_{si}kT+C_{ox}qR(V_{gs}-\Delta\varphi-\phi_{SL})}{4\varepsilon_{si}kT+C_{ox}qR(V_{gs}-\Delta\varphi-\phi_{SS})}\right]\right]. \quad (35)$$

According to the surface potential Equation (10), this drain expression can be simplified into

$$I_{ds} = \mu\frac{\pi R^2}{L}n_i kT e^{q(V_{gs}-\Delta\varphi)/kT}(1-e^{-qV_{ds}/kT}). \quad (36)$$

The sub-threshold current in (36) is proportional to the cross-section area of the SRG MOSFET and independent of t_{ox}. This is a characteristic of the volume inversion effect that cannot be captured by the standard charge-sheet based models.

iii) *Saturation region*. This regime occurs when the contribution of the drain end is little to the drain current. Hence, the drain current is expressed as

$$I_{ds} = \mu\frac{\pi R}{L}\left(Q_S+\frac{4C_{ox}kT}{q}\right)(\phi_{SL}-\phi_{SS}). \quad (37)$$

The saturation current mainly depends on the source inversion charge density as expected for a bulk MOSFET.

In order to verify the presented drain current model, the comparison of drain current curves between the model prediction and the three-dimensional simulation is also performed as done for the surface potential and inversion charge. Figure 4 shows the SRG MOSFET transfer characteristics. As analysed above on (36), sub-threshold current of the $R = 20$ nm device is almost 16 times as large as that of the $R = 5$ nm device. The current ratio is exactly equal to the square of the radius ratio. While for the strong inversion current, e.g. the turn on current at $V_{gs} = 2$ V, the current ratio is in accordance with the radius ratio, as expected from (34). The volume inversion effect of SRG MOSFET demonstrated in Figure 4 is well described by the presented model, matching the three dimension numerical simulation. Figure 5 plots the SRG-MOSFET output characteristics, calculated from the surface potential-based model and the three dimension numerical simulation. Again, good agreements are observed without using any fitting parameters.

Figure 6 shows the analytical terminal charges versus V_{ds} curves from the presented model (curves) with two V_{gs}

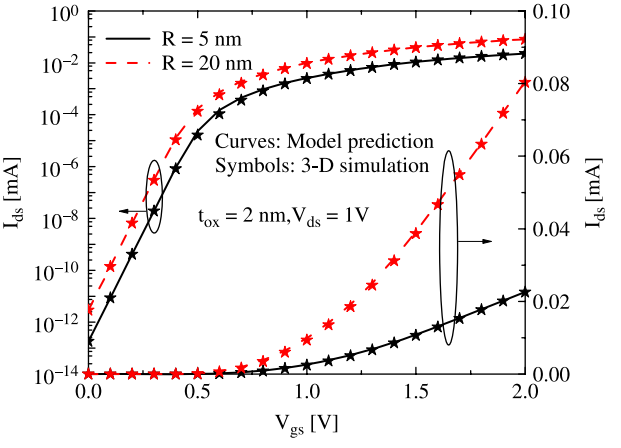

Figure 4. Transfer characteristics obtained from the surface potential-based drain current model for two silicon film radii (solid and dashed curves), compared with three dimension numerical simulations from Sentaurus (symbols).

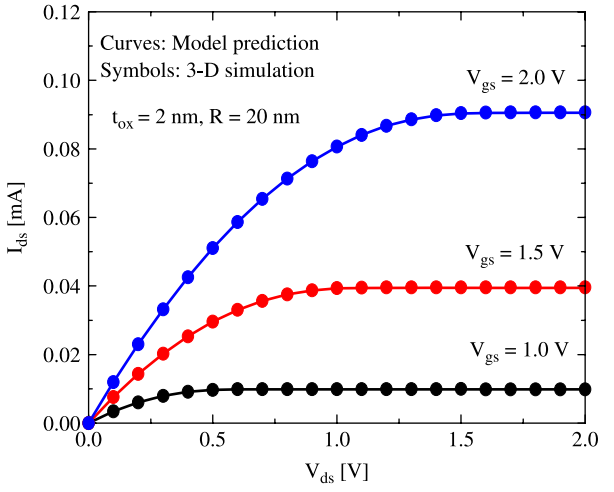

Figure 5. Output characteristics obtained from the surface potential-based drain current model (solid curves) compared with three dimension numerical simulations from Sentaurus (symbols).

conditions, compared with results from the three-dimensional simulation (symbols). Calculations of the terminal charges shows a ~2–3% difference between the numerical simulation and analytical model. Here, the symmetry of the source and drain charges for $V_{ds} = 0$ is shown in Figure 6. An interesting result is that the source charge approaches 6/10 of the gate charge while the drain charge approaches 4/10 of the gate charge when the nanowire SRG MOSFET enters the saturation region. The difference of the gate voltage changes the magnitude of the source and drain charges while they eventually approach their saturation ratio value.

Non-reciprocal trans-capacitance is an important but difficult compact modelling issue. The traditional Meyer

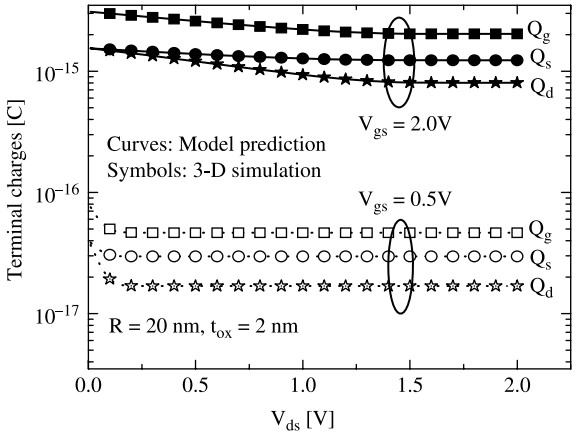

Figure 6. Terminal charge versus V_{ds} for two different V_{gs} obtained from the analytic model (solid and dot curves), compared with the three-dimensional simulation (symbols).

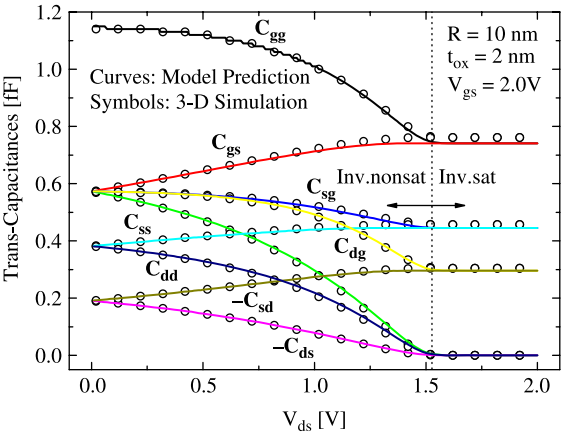

Figure 7. Model predicted trans-capacitances versus drain voltage for $V_{gs} = 2\,V$, compared with the three-dimensional device simulation.

reciprocal trans-capacitance model leads to convergence issues and non-conservation charge. Figure 7 illustrates the calculated trans-capacitances versus drain voltage in comparison with three dimension numerical simulation. Again, an excellent agreement is found in the figure. The symmetry of the trans-capacitances such as the source-gate C_{sg} and the drain-gate C_{dg} for $V_{ds} = 0$ is again preserved by the analytic model. In addition, a direct comparison from Figure 7 shows that the trans-capacitance pairs C_{sg}, C_{gs} and C_{dg}, C_{gd}, are generally different, confirming the non-reciprocal characteristics. This result is consistent with the MOSFET device physics.

Since the nanowire SRG MOSFET is a three-terminal device, the physics based gate, source and drain terminal trans-capacitances are important for circuit simulation. Figure 8 plots the corresponding trans-capacitance versus

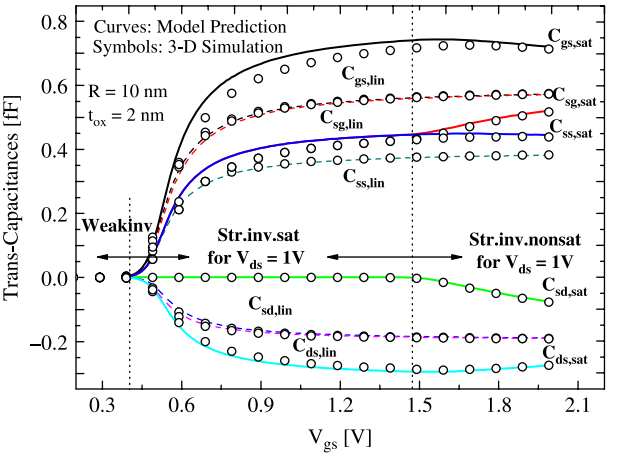

Figure 8. Model predicted trans-capacitances versus gate voltage for two different drain voltage $V_{ds} = 0\,V$ and $V_{ds} = 1\,V$, compared with the three-dimensional device simulation.

V_{gs} curve, obtained from the analytic model (solid curves) and three dimension numerical simulation (symbols) for $V_{ds} = 0\,V$ and $V_{ds} = 1\,V$. Both the model and the simulation show that the source terminal trans-capacitances always satisfy the trans-capacitance relationship, as shown in Equations (28–30). On the other hand, the trans-capacitance pairs between C_{sd}, C_{ds} and C_{dg}, C_{gd} are quite different as a result of the non-reciprocal characteristics of the SRG MOSFETs, although the physics based C_{sd} and C_{ds} are always negative due to the electrostatic feedback effects while they are very small compared with others. The trans-capacitance model shows a good agreement with the numerical simulation.

4. Conclusions

In summary, we have presented an analytical surface potential-based non-charge sheet core model suitable for compact modelling of intrinsic nanowire SRG MOSFETs. From Poisson–Boltzmann equation in the cylindrical structure, the surface potential equation is derived. Based on the exact solution of the surface potential at the source and drain ends, the drain current model is obtained from Pao–Sah's dual integral model. The trans-capacitance model is also obtained within the surface potential-based frame. All the operation regions and the transitions are correctly described by preserving the physics in the proposed model. In particular, the volume inversion effect that cannot be captured by using the traditional charge-sheet approximation is well accounted for in this model. The proposed model is verified by three dimension numerical simulation, and good agreements between both are observed.

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